

FIG. 1

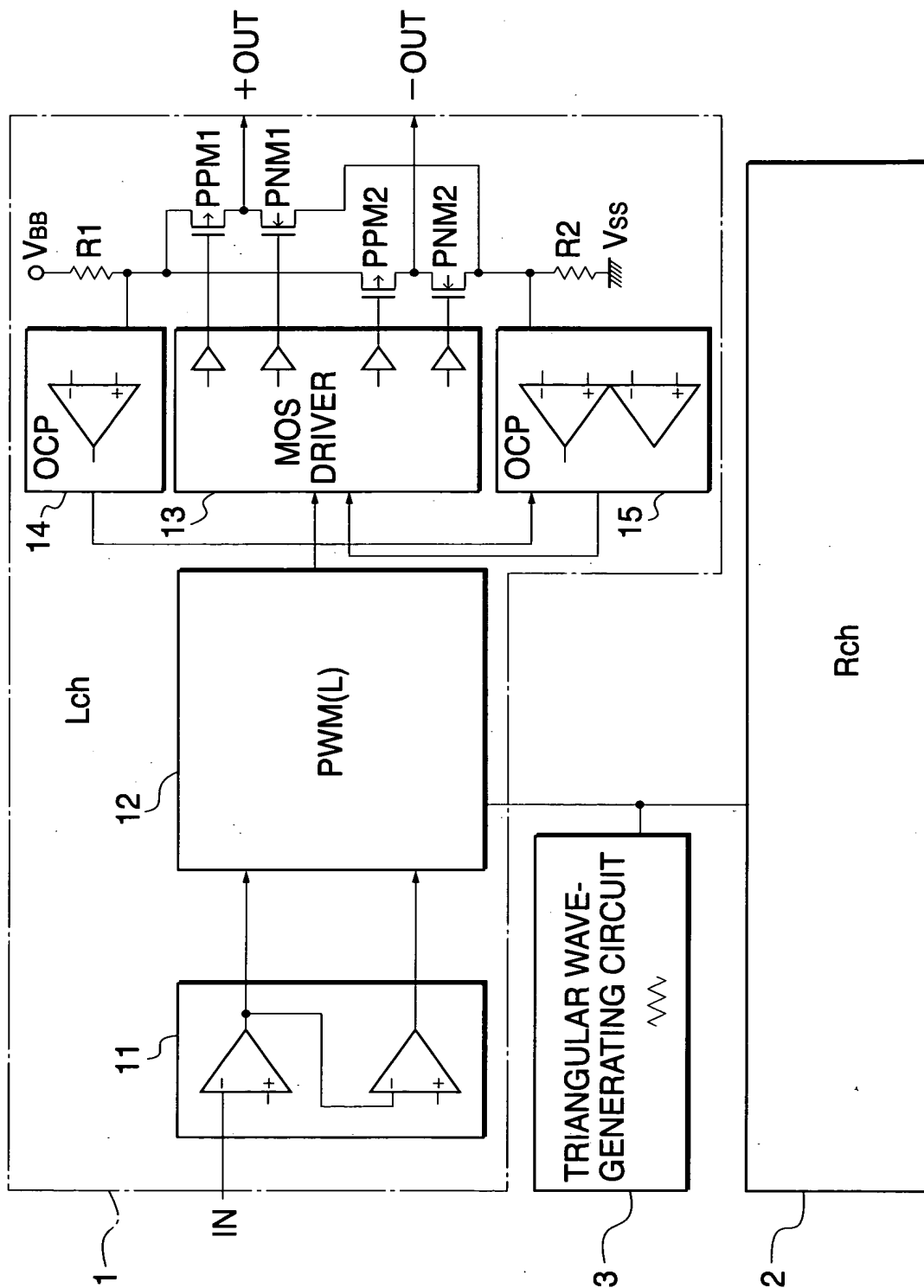
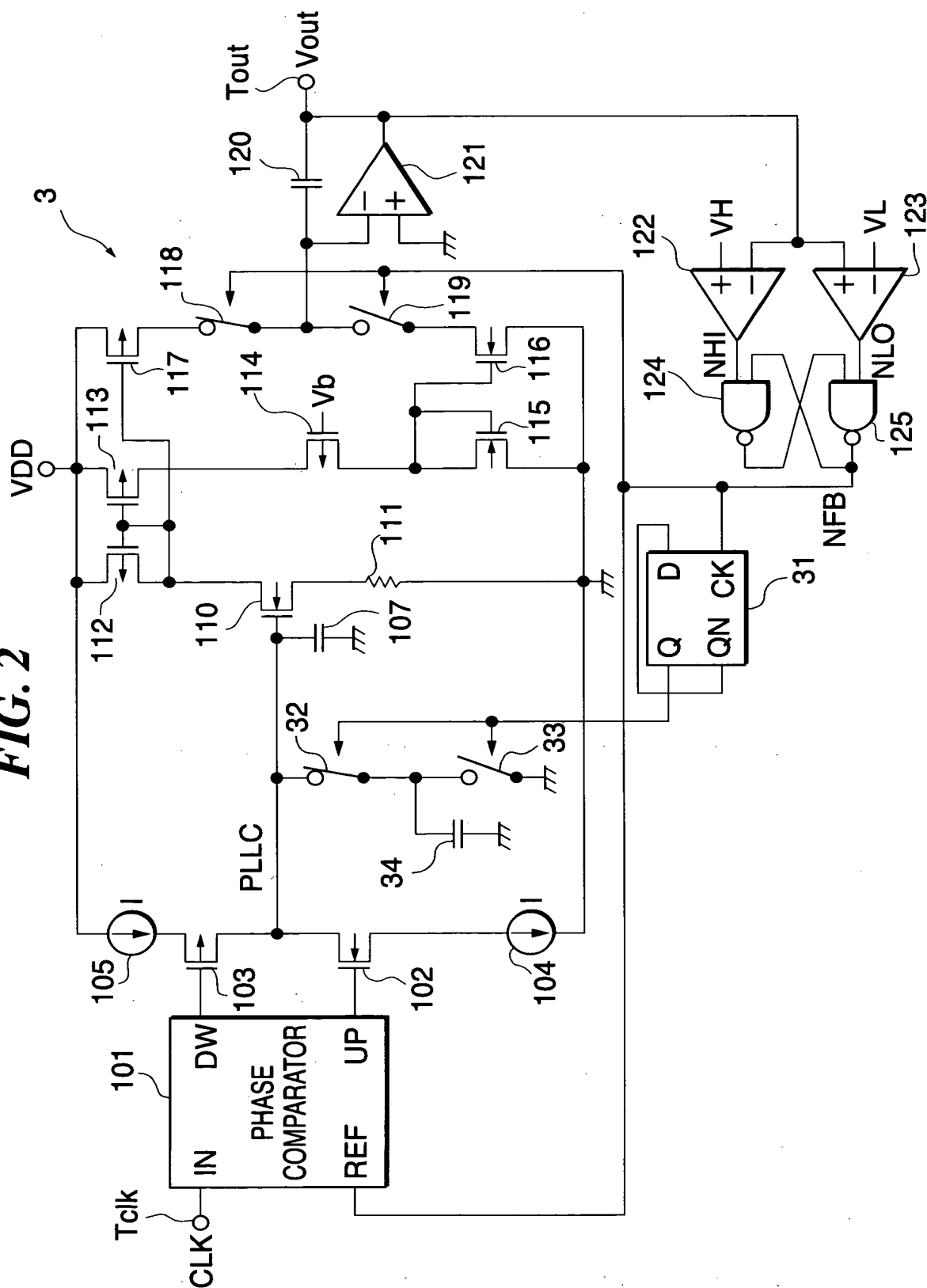


FIG. 2



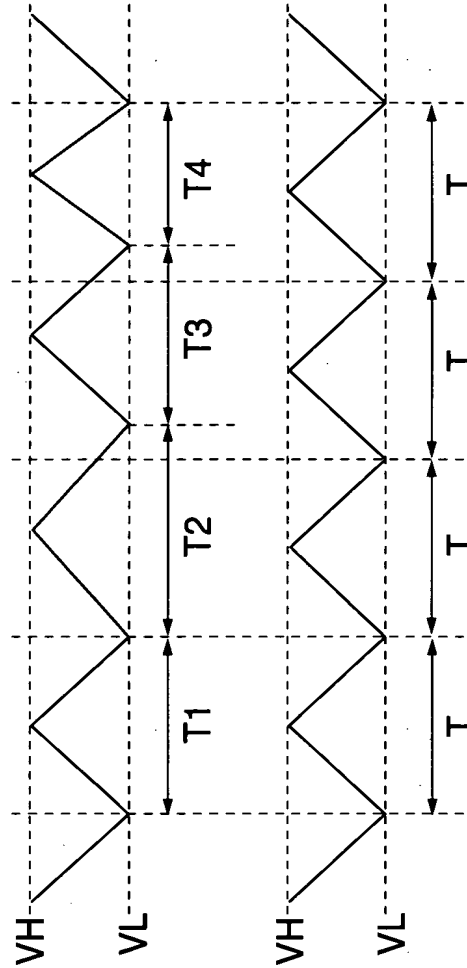


FIG. 3A

FIG. 3B

FIG. 4

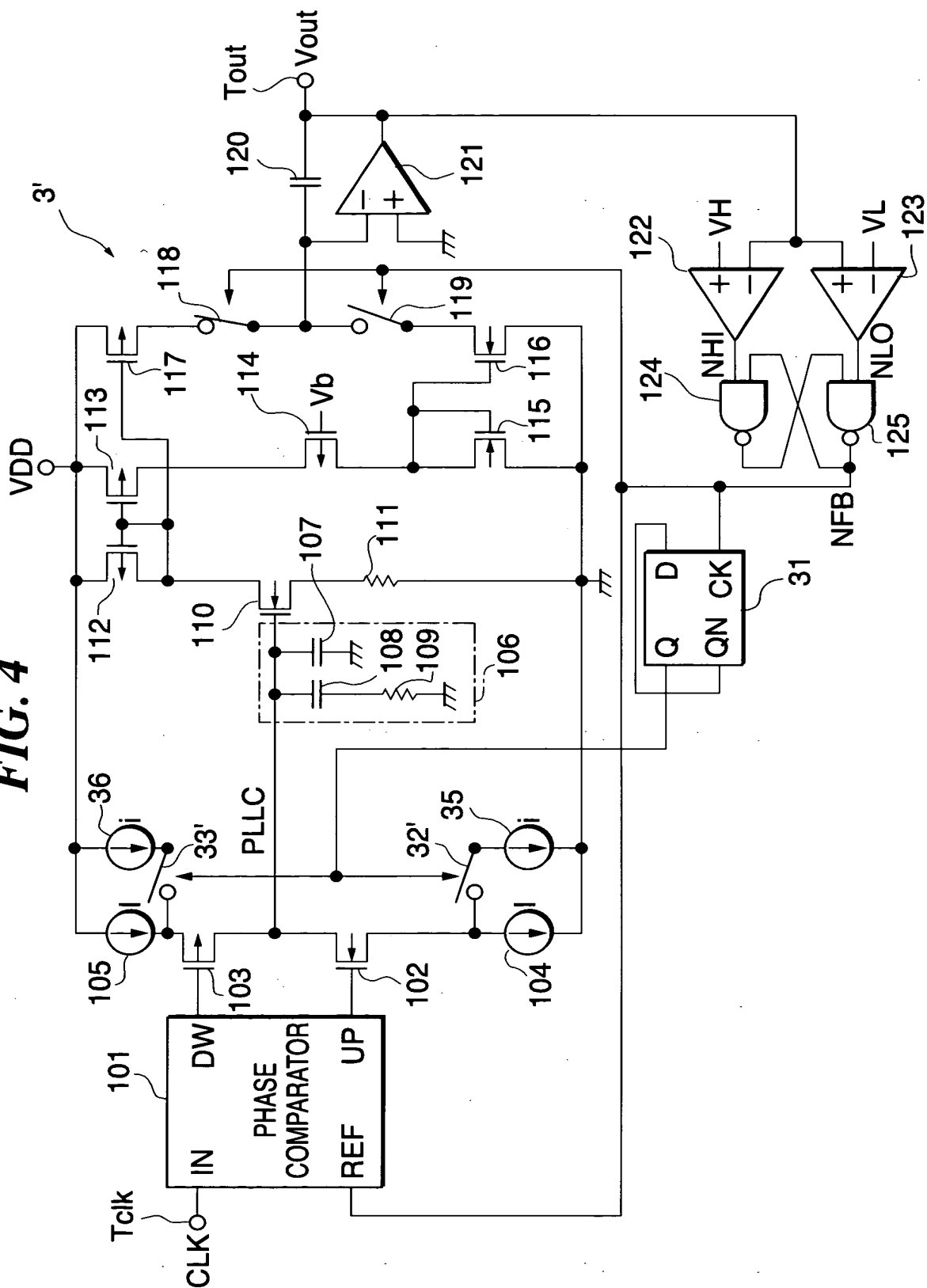
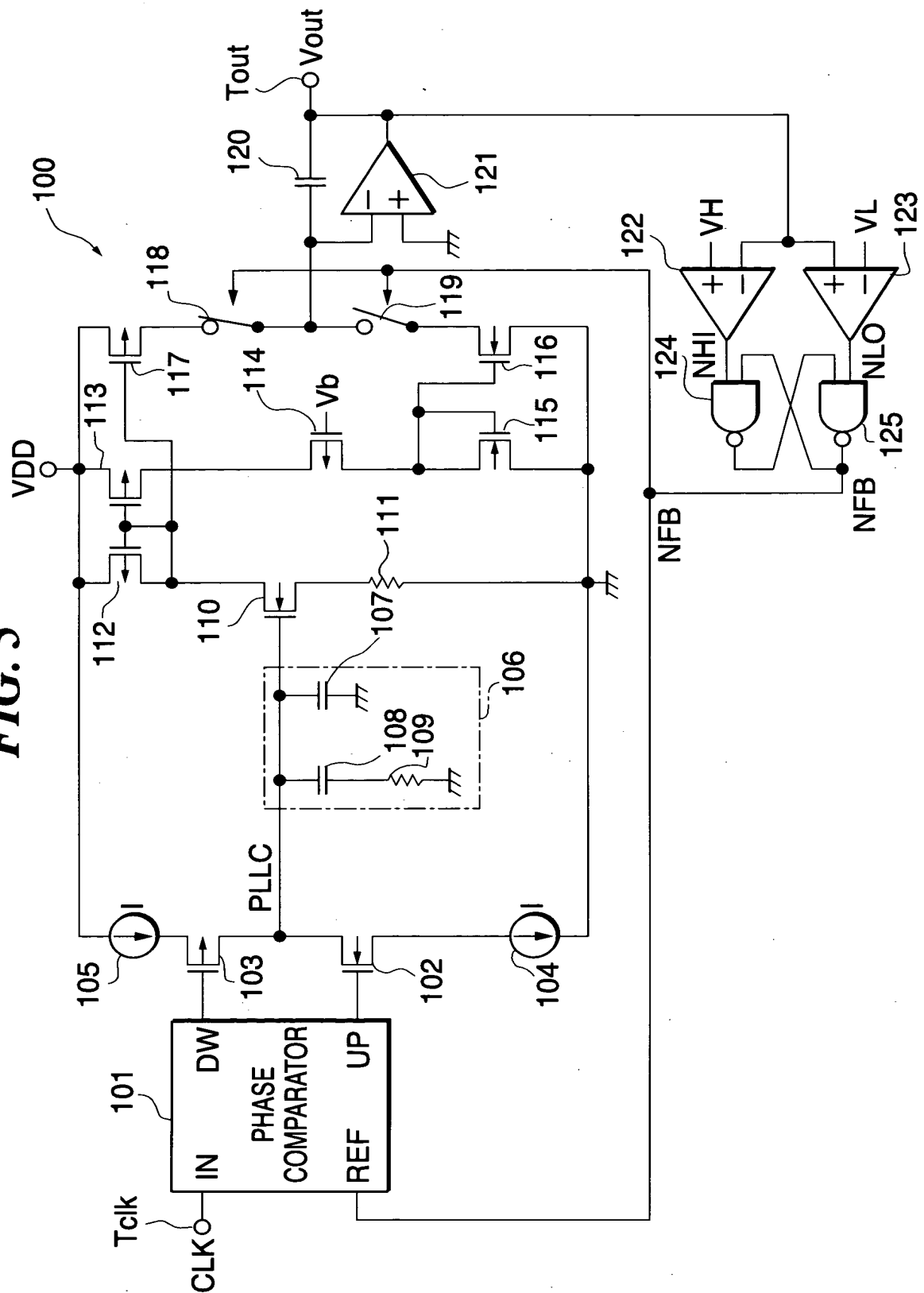


FIG. 5



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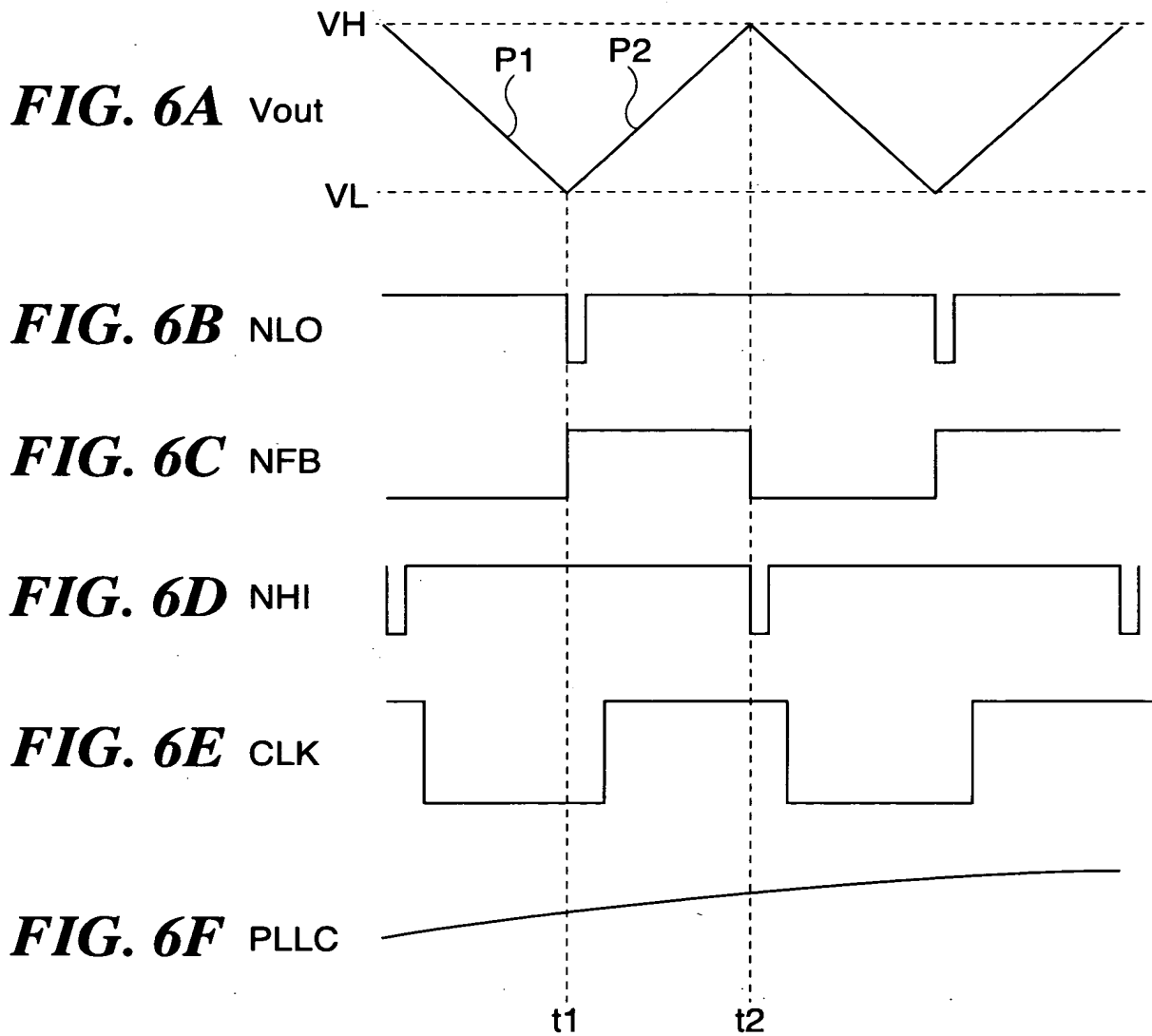


FIG. 8

The diagram illustrates a PLL system (5) with the following components and connections:

- Phase Comparator (101):** Receives **Tclk** at the **IN** terminal and **CLKO** at the **REF** terminal. It has control inputs **DW** and **UP**. Its output is connected to the **PLL** input of the **PLLC** block (102).
- PLLC (102):** A phase-locked loop controller that outputs a control signal to the **PLLC** input of the **PLLC** block (103).
- PLLC (103):** A phase-locked loop controller that outputs a control signal to the **PLLC** input of the **PLLC** block (104).
- Current Sources (104, 105):** Two current sources, labeled **I**, providing bias currents to the circuit.
- Transistors (106, 107, 108, 109):** A network of transistors and capacitors forming the core of the PLLC, with nodes labeled **106**, **107**, **108**, and **109**.
- Resistors (110, 111, 112, 113, 114, 115, 116):** A network of resistors connected to the transistors and current sources.
- Capacitors (117, 118, 119):** A network of capacitors connected to the transistors and resistors.
- Output Stage (120, 121):** A buffer or driver stage consisting of a transistor (120) and an op-amp (121) that produces the final output **Vout** at the **Tout** terminal.
- Feedback Loop (122, 123, 124, 125):** A feedback network including a divider (122), a phase shifter (123), and a feedback filter (124, 125) that feeds back the output to the **REF** input of the phase comparator.

